When simulating or synthesizing in Vivado you may be asked to find the errors in elaborate.log or xvlog.log. You can find these files the directory: <project>\<project>.sim\sim\_1\behav\xsim

elaborate.log Contains errors related to instantiating components

 xvlog.log Contains errors related to syntax

When Vivado complains that it cannot find a file that you have added, delete all the files in:

<project>\<project>.sim\sim\_1\behav\xsim\xsim.dir\xil\_defaultlib

File system errors

 Never put spaces in directory or file names

 Path + filename cannot exceed 260 characters!

[IP\_Flow 19-4995] The host OS only allows 260 characters in a normal path. The IP cache path is more than 80 characters. If you experience issues with IP caching, please consider changing the IP cache to a location with a shorter path. Alternately consider using the OS subst command to map part of the path to a drive letter.

Current IP cache path is c:/users/chris/dropbox/mycourses/eeng498/vhdl\_fall2023/lab04 oscilloscope hardware/lab04 oscilloscope hardware.tmp/acquirewithhdmi\_v1\_0\_project/acquireWithHDMI\_v1\_0\_project.cache/ip

Not sure how to handle this one yet….

[IP\_Flow 19-626] File Group 'xilinx\_vhdlsynthesis (VHDL Synthesis)': verilogSource subcore file "hdl/encode.v" is referenced from the pure language VHDL file group. Please consider changing the file group type to support mixed language sources.

**Symptom: VITIS does not have library files for your IP**

You have an existing Vitis project using an XSA file created in Vivado. This XSA file is a combination of the Zynq and custom IP. You have gone back in an re-edited the custom IP. Updated the IP Repo, re-generated product terms, generated the generated bitstream and then exported hardware. Back in Vitis you update the hardware specification. Then trying to compile you get an error that myCustomIP.h file is not found. Especially after updating your custom IP, check it has been assigned an address using the Address Editor tab. The image below is from Vivado and shows that the acquireWithHDMI module was not being assigned an address in the memory space of the Zynq. I added a second instance which was assigned an address :/

You cannot find the IP in the following folders:

* Vitis\oscilloscope\_workspace\oscilloscopeHardware\_wrapper\zynq\_fsbl\zynq\_fsbl\_bsp\ps7\_cortexa9\_0\libsrc
* Vitis\oscilloscope\_workspace\oscilloscopeHardware\_wrapper\ps7\_cortexa9\_0\standalone\_ps7\_cortexa9\_0\bsp\ps7\_cortexa9\_0\libsrc

In Vivado, right click on custom IP and select assign. Bingo!



I fixed the issues by right clicking on the unassigned IP and select Assign to fix this problem.

**Symptom: VIVADO forgets where src folder are**

While re-packaging IP because of errors, the IP seems to have forgotten where some of the files are. But this doesn’t make sense because they are in the src folder associated with the IP???





In order to fix this situation, you will need to FORCE the inclusion of the files. To accomplish this you will need to work with the TCL counsel at the bottom of the screen. First try to add the IP back as follows:

* Go to your Sources area, right click on Design Sources, then specify Add Sources
* In the Add Sources pop-up, select Add or Create Design Sources, click Next
* In the Add Sources pop-up, click Add Files
* In the Add Files pop-up, navigate to ipRepo/<repoName>/src/<instanitateIP>/<instantiateIP>.xci
* This should generate an error pop-up. Click Ok to dismiss it.

The real goal of this is to copy the TCL command used to add the instantiateIP repo. In our case the blue text below.

add\_files -norecurse -copy\_to c:/Users/chris/Dropbox/Mycourses/EENG498/VHDL\_fall2023/ip\_repo/acquireWithHDMI\_1\_0/src C:/Users/chris/Dropbox/Mycourses/EENG498/VHDL\_fall2023/ip\_repo/acquireWithHDMI\_1\_0/src/blk\_mem\_gen\_0/blk\_mem\_gen\_0.xci

ERROR: [Vivado 12-3629] The destination directory 'c:/Users/chris/Dropbox/Mycourses/EENG498/VHDL\_fall2023/ip\_repo/acquireWithHDMI\_1\_0/src/blk\_mem\_gen\_0' already exists, please use -force if you want to overwrite!

Copy the blue add\_files command and then paste it in the TCL command area. Add add -force just after the add\_force command. Hit return and whamo, you’re back in business.



**Symptom: The acquisition cycle “hangs” a-periodically.**

The time required to read the AD7606 is longer than the sampling interval setup by the counters in the datapath. There are no safeguards against this at the present time.

Solutions:

* A status word bit that indicates this and pump it out to a, sticky, LED that indicates this error. I am not sure if environmental factors influence the conversion time of the AD7606.
* Adjustable sampling rate. This is already present in the datapath, but the control bits of the sampling rate mux (which selects the rate) are hardwired for the fastest rate. Pushing these control bits out to the ARM would allow the ARM to select a slower rate as needed.